IN THE CLAIMS

Please amend the following claims:

1. – 11. (Cancelled)

12. (Currently Amended) ~~The~~ A method ~~of claim 9~~ for implementing a design verification system into at least one programmable logic device so that a user design to be verified can be implemented therein, comprising:

mapping the user design into operations for execution;

partitioning each of said operations into processor types suitable for each of said operations, wherein the processor types comprise logic processors, macro processors, memory processors and general purpose processors;

ordering each of said processor types according to connectivity of each of said processor types;

scheduling communications between each of said processor types; and

programming said at least one programmable logic device to implement said processor types;

wherein said logic processors comprise:

an instruction memory;

a logic functional unit that executes Boolean logic instructions; and

a register file controlled by said instruction memory, said register file having outputs selectively in communication with said logic functional unit, said register file

comprised of input registers and local registers, said local registers in communication with output from said logic functional unit.

13. (Currently Amended) ~~The~~ A method ~~of claim 9~~ for implementing a design verification system into at least one programmable logic device so that a user design to be verified can be implemented therein, comprising:

mapping the user design into operations for execution;

partitioning each of said operations into processor types suitable for each of said operations, wherein the processor types comprise logic processors, macro processors, memory processors and general purpose processors;

ordering each of said processor types according to connectivity of each of said processor types;

scheduling communications between each of said processor types; and

programming said at least one programmable logic device to implement said processor types;

wherein said macro processors comprise:

an instruction memory;

a macro processor executes macro instructions; and

a register file controlled by said instruction memory, said register file having outputs selectively in communication said macro functional unit, said register file comprised of input registers and local registers, said local registers in communication with output from said macro functional unit.

14. – 17. (Cancelled)

18. (Currently Amended) ~~The~~ A method ~~of claim 17~~ for verifying functionality of an electronic design, the electronic design including Boolean logic gates, at least one macro function and at least one memory circuit, comprising;

compiling the electronic design into logic processors that execute the Boolean logic gates, at least one macro processor that executes the at least one macro function, at least one memory processor that executes the at least one memory circuit, and an interconnect architecture that interconnects said logic processors, said at least one macro processor and said at least one memory processor to one another;

programming said at least one programmable logic device to implement said logic processors, said at least one macro processor and said at least one memory processor;

applying stimulus to said logic processors, said at least one macro processor and said at least one memory processor such that said logic processors execute the Boolean logic gates, said at least one macro processor executes the at least one macro function and said at least one memory processor executes the at least one memory circuit; and

collecting output responses generated by said logic processors, said at least one macro processor programmed and said at least one memory processor;

wherein said interconnect architecture further comprises:

an instruction memory;

a plurality of buffers, wherein the number of said plurality buffers is equal to ~~the~~ a sum of the number of said logic processors added to ~~the~~ a number of said at least one macro processor added to ~~the~~ a number of at least one said memory processor, each of said plurality of buffers having an output that is selected by said instruction memory;

a plurality of selectors, wherein the number of said plurality of selectors is equal to the number of said plurality of buffers, each of said plurality of selectors in communication with each of said plurality of buffers so that data stored in any of said plurality of buffers can be transmitted to any of said plurality of selectors, each of said plurality of selectors controlled by said instruction memory; and

a plurality of output ports, each of said plurality of output ports corresponding to one of said plurality of selectors.

19. – 20. (Cancelled)

21. (Currently Amended) ~~The~~ A method ~~of claim 17~~ for verifying functionality of an electronic design, the electronic design including Boolean logic gates, at least one macro function and at least one memory circuit, comprising:

compiling the electronic design into logic processors that execute the Boolean logic gates, at least one macro processor that executes the at least one macro function, at least one memory processor that executes the at least one memory circuit, and an interconnect architecture that interconnects said logic processors, said at least one macro processor and said at least one memory processor to one another;

programming said at least one programmable logic device to implement said logic processors, said at least one macro processor and said at least one memory processor;

applying stimulus to said logic processors, said at least one macro processor and said at least one memory processor such that said logic processors execute the Boolean logic gates, said at least one macro processor executes the at least one macro function and said at least one memory processor executes the at least one memory circuit; and

collecting output responses generated by said logic processors, said at least one macro processor programmed and said at least one memory processor;

wherein said logic processors comprise:

an instruction memory;

a register file controlled by said instruction memory, said register file having outputs selectively in communication said logic functional unit, said register file comprised of input registers and local registers, said input registers in communication with said interconnect architecture, said local registers in communication with output from said logic functional unit.

22. (Currently Amended) ~~The~~ A method ~~of claim 17~~ for verifying functionality of an electronic design, the electronic design including Boolean logic gates, at least one macro function and at least one memory circuit, comprising;

compiling the electronic design into logic processors that execute the Boolean logic gates, at least one macro processor that executes the at least one macro function,

at least one memory processor that executes the at least one memory circuit, and an interconnect architecture that interconnects said logic processors, said at least one macro processor and said at least one memory processor to one another;

programming said at least one programmable logic device to implement said logic processors, said at least one macro processor and said at least one memory processor;

applying stimulus to said logic processors, said at least one macro processor and said at least one memory processor such that said logic processors execute the Boolean logic gates, said at least one macro processor executes the at least one macro function and said at least one memory processor executes the at least one memory circuit; and

collecting output responses generated by said logic processors, said at least one macro processor programmed and said at least one memory processor programmed into said at least one programmable logic device;

wherein said at least one macro processor comprises:

an instruction memory; and

a register file controlled by said instruction memory, said register file having outputs selectively in communication said macro functional unit, said register file comprised of input registers and local registers, said input registers in communication with said interconnect architecture, said local registers in communication with output from said macro functional unit.

23. (Cancelled)

24. (New) The method of claim 12 wherein said partitioning step comprises:

consulting a programmable logic device library that has a preprogrammed mix of said processor types; and

selecting an appropriate preprogrammed mix of said processor types for said operations for execution.

25. (New) The method of claim 12 wherein said scheduling step comprises:

creating a program for instruction memories within each of said processor types; and

creating programming files for each programmable logic device used for verifying the user design.

26. (New) The method of claim 12 further comprising loading said program into each of said instruction memories.